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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,620	12/15/2003	Mitsuhiko Ogihara	MAE 303	2032

23995 7590 12/23/2005

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,620	OGIHARA ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *17-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 14-16* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated November 14, 2005, Applicant has elected without traverse the Invention of Group I, Claims **1-16**, drawn to a semiconductor apparatus is acknowledged. Accordingly, Claims **17-21** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected Claims **17-21**.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in JAPAN, 2002-371769 on 12/24/2002.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 12/15/2003. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims **1, 5-9 and 14-16** are rejected under 35 U.S.C. 102(a) as being anticipated by Taninaka et al. (USP 6,388,696).

Regarding Claims **1, 14 and 15**, Taninaka et al. disclose in Figs. 3-16, and the corresponding texts as set forth in column 8, line 45-column 14, line 49, a semiconductor apparatus comprising:

a substrate 102;

m electrically conductive layers 113 formed on said substrate, m being an integer of 2 or more, potentials of said m electrically conductive layers being capable of being independently controlled; and

semiconductor thin films including at least one semiconductor device/LED 110 respectively, said semiconductor thin films being bonded on surfaces of said m electrically conductive layers respectively.

Regarding Claims **5-9**, Taninaka et al. disclose number of said semiconductor thin films is m, and said m semiconductor thin films are bonded on said m electrically conductive layers respectively in a one-to-one correspondence; wherein ends of said electrically conductive layers in a row direction of said semiconductor devices and ends of said semiconductor thin films in a row direction of said semiconductor devices are located on imaginary reference planes perpendicular to a surface of said substrate in such a way that said ends of said electrically conductive layers and said ends of said semiconductor thin films are in alignment, number of said semiconductor devices is n for each of said semiconductor thin films, n being an integer of 2

or more, number of said semiconductor thin films bonded on said m electrically conductive layers is n for each of said electrically conductive layers, n being an integer of 2 or more, and number of said semiconductor device formed in each of said n semiconductor thin films is 1 (Figs. 3-4).

Regarding Claim **16**, Taninaka et al. disclose said electrically conductive layers are made of any of metal and polysilicon (col. 35, lines 28-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Taninaka et al. (USP 6,388,696) in view of JP 10-063807.

Taninaka et al. disclose the substrate being a semiconductor/insulating substrate except for the semiconductor further comprising an integrated circuit device formed in or disposed on the substrate. JP 10-063807 discloses in Fig. 1 the semiconductor comprises an integrated circuit device formed in or disposed on a substrate used to process an electric signal. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include an integrated circuit device formed in or disposed on the substrate to process electric signals as taught by JP 10-063807 as set forth in the English Abstract.

Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Taninaka et al. (USP 6,388,696) in view of Ogihara et al. (USP 6,313,483 hereinafter referred to as "Ogihara'483".

Taninaka et al. disclose all the claimed limitations except for said semiconductor device includes a first-conductive-type semiconductor layer and a second-conductive-type semiconductor layer, a conductive-type of said second-conductive-type semiconductor layer being different from a conductive-type of said first-conductive-type semiconductor layer, and said first-conductive-type semiconductor layer being in contact with said electrically conductive layer. Ogihara'483 teaches in Fig. 1 that said semiconductor device/LED includes a first-conductive-type/n-type semiconductor layer 12 and a second-conductive-type/p-type semiconductor layer 14, a conductive-type of said second-conductive-type/p-type semiconductor layer being different from a conductive-type of said first-conductive-type/n-type semiconductor layer. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a semiconductor device/LED including a first-conductive-type/n-type semiconductor layer and a second-conductive-type/p-type semiconductor layer, a conductive-type of said second-conductive-type/p-type semiconductor layer being different from a conductive-type of said first-conductive-type/n-type semiconductor layer to form a pn junction where light is emitted by radiative recombination of electrons and holes in the vicinity of the pn junction (col. 1, lines 9-24).

Allowable Subject Matter

Claims **10-13** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art of record, taken alone or in combination, fails to teach or render obvious the semiconductor apparatus further comprising: m common wiring lines disposed on said substrate, potentials of said m common wiring lines being capable of being independently controlled, said m common wiring lines being electrically connected to said m electrically conductive layers in a one-to-one correspondence; and n signal wiring lines disposed on said substrate, potentials of said n signal wiring lines being capable of being independently controlled; wherein said n second-conductive-type semiconductor layers disposed on each of said m electrically conductive layers are electrically connected to said n signal wiring lines so that k-th one of said n second-conductive-type semiconductor layers and k-th one of said n signal wiring lines are electrically connected in a one-to-one correspondence, k being an integer between 1 and n as recited in Claim **10**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Andy Huynh

Patent Examiner